Scaling down and stacking up: how the trends in semiconductors are affecting chemical-mechanical planarization (CMP)

Wei-Tsu Tseng
IBM Semiconductor Technology Research
257 Fuller Road, Albany, NY 12203, USA
Tel.: +1-914-299-7479, E-mail: wei-tsu.tseng1@ibm.com

Over the past 5+ decades, the semiconductor industry has been following the Moore's law, which perceives that roughly every 2 years, the number of transistors on microchips will double, while the cost of computers is halved. The law itself has been driving the advancement of industry to achieve increased speed and capability with lower cost of ownership. Inevitably, the law translates to the areal scale-down of devices and macros in each new technology nodes as shown in Fig. 1.

An emerging trend in the industry began 10+ years ago, when demands for higher device functionality and constraints of areal scaling eventuated the innovation of 3D devices as illustrated in Fig. 2.

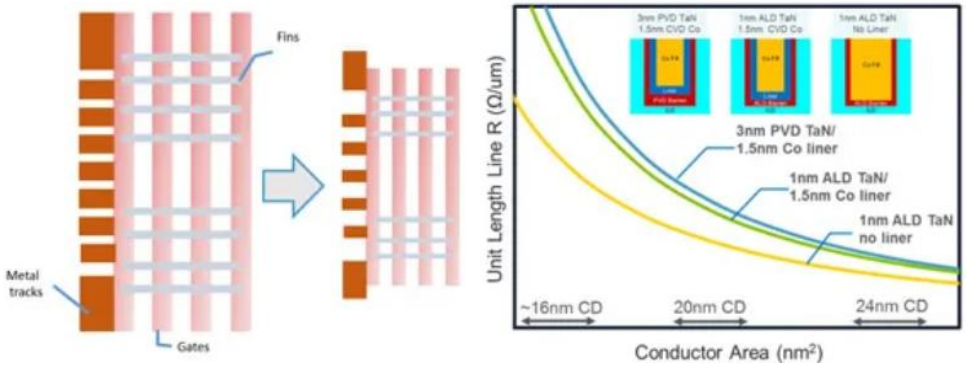

Fig. 1. Scaling down of semiconductors: Gate area scaling (*left*)**; Cu interconnects scaling** (*right*).

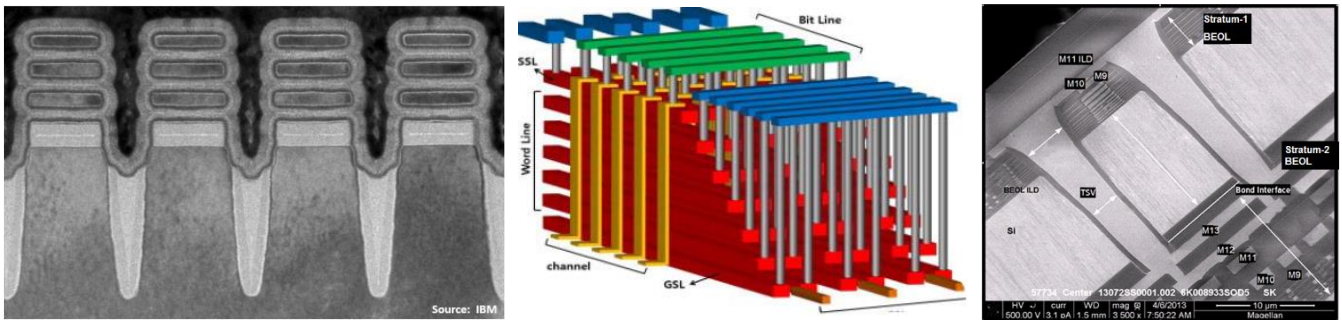

Fig. 2. Stacking up of semiconductors: Nanosheets (*left*)**; 3D NAND** (*center*)**; W2W 3D bonding** (*right*)**.**

Consequently, semiconductors are scaling down and stacking up at the same time: device feature size is shrinking in the x-y plane, while even more layers of materials are being processed in the z- direction. Such aggressive geometric driving force engenders a multitude of challenges to process technologies like CMP. First, it increases the number of CMP steps inevitably; second, it calls for the necessity of CMP for new materials (e.g., new work function metals for gates, new barrier/liner for Cu interconnects) to meet the required specifications; and thrid, the tolerance for non-uniformity, variabiity, and defectivity become even more stringent than ever.

In general, the 3 main CMP performance metrics, planarity, uniformity, and defectivity are being stretched to meet the specs down to nm scale on one hand, while still required to polish 3D stacks on the order of μm on the other. Such critical challenges call for innovations in HW/SW such as more robust end-point, APC/AI-based control…etc.; in consumables such as higher slurry selectivity, higher pad planarzation efficiency in varying length scales, and more effective cleaning chemistry..etc. In this contribution, the CMP challenges and potential solutions in the era of aggressive semiconductror scaleing and stacking will be reviewed and projected.