Metrology and Inspection Challenges with EUV patterning at advanced nodes

Sandip Halder

imec Kapeldreef 75, Heverlee B3001, Belgium

As we strive to keep Moore's law alive, devices continuously shrink in size and processes become more complex. To monitor and control these advanced processes, complicated metrology, inspection and data analysis methods are required. With the adoption of EUV in logic and recently in memory device manufacturing there is a path to continue scaling further but it comes with its own challenges.

The adoption of new device architectures like GAA, Nanosheets, CFET's which are 3D brings its own set of challenges. Chipmakers use different tools and methods for process control like optical inspection and metrology, x-ray metrology and e-beam inspection and metrology to characterize processes and improve yields. With new device architectures and devices, new materials are also added to the manufacturing process. Finding the root cause of random as well as systematic defects fast and reliably is of utmost importance. The minimum defect size which can be a yield limiter keep scaling from node to node and is currently below 10nm for most tight design rule process layers. Detection capabilities on such small defects relies on having good signal to noise ratio which is also becoming challenging with smaller defects. Advances in design-based inspection have gained a lot of importance in noise suppression in optical inspection tools which cannot resolve the underlying pattern. AI and ML approaches have gained a lot of importance on optical metrology tools. In these tools, measurement of overlay and CD is key to achieving EPE and other yield requirements at fast throughput for in-line applications with high in-die and across wafer sampling. The mask itself which is being used to print the features have become more complicated. Process control of mask manufacturing and inspection is also critical to avoid yield detractors. Speaking of big data environment, there is a massive volume data that a fab generates from the different tool systems. Hybrid metrology is often mentioned to be the way forward.

To continue patterning scaling to smaller pitches and CDs, next generation EUV systems are being built with High NA optics. These EUV tools require thinner resists and UL's, anamorphic mask designs among other infrastructure changes and brings in additional challenges for metrology and inspection. Even with SEM resolution, contrast can be very poor depending on the type and thickness of resist and underlayers. Various deep learning-based methods have been developed to denoise and extract more accurate measurements. Also, in the field of inspection and defect classification the use of AI has helped tremendously. In this talk we will focus on some of these key challenges and developments with EUV based patterning at advanced nodes.