Mitsumasa Koyanagi

(Tohoku University, Japan)

Mitsumasa Koyanagi was born in Hokkaido, Japan on 1947. He received Ph.D. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1974. He joined the Central Research Laboratory, Hitachi Ltd. in 1974 where he worked on research and development of MOS memory device and process technology and invented a stacked capacitor DRAM memory cell which has been widely used in the DRAM production. Stacked capacitor DRAM cell was the first commercialized 3D device employed in LSI. In 1985, he joined the Xerox Palo Alto Research Center, California where he worked on research and development of sub-micron CMOS devices, poly-silicon thin film transistors and the design of analog/digital LSIs. In 1988 he joined the Research Center for Integrated Systems, Hiroshima University, as a professor where he worked on sub-0.1um MOS devices, device modeling, poly-Si TFT devices, 3D integration technology, optical interconnection and parallel computer system specific for scientific computation. He fabricated the smallest MOS transistor with a gate length of 70nm at that time which was presented in IEEE IEDM 1992. He proposed three-dimensional integration technology based on wafer-to-wafer bonding and Through-Si Via (TSV) for the first time in 1989. Since 1994, he has been a professor in Intelligent System Design Lab., Department of Machine Intelligent and Systems Engineering (from 1994 to 2003) , in Advanced Bio-Nano Devices Lab., Department of Bioengineering and Robotics, Graduate School of Engineering (from 2003 to 2010), and in New Industry Creation Hatchery Center (NICHe) (from 2010 to date), Tohoku University where his interests were 3D integration technology, optical interconnection, nano-CMOS devices, memory devices, parallel computer system, retinal prosthesis chip, brain-machine interface (BMI) and neural prosthesis chip and AI chip. He established a small production line for 3D integration using 12-inch wafers called GINTI (Global Integration Initiative) in 2013 and became a director. Currently he is a senior research fellow in New Industry Creation Hatchery Center (NICHe), Tohoku University and his current interests are focused on 3D integration technology. He was a Distinguished Professor in Tohoku University.

He has published more than 400 technical papers and given more than 200 invited talks. He was awarded IEEE Jun-ichi Nishizawa Medal, IEEE Cledo Brunetti Award, SSDM (Solid-State Devices and Materials) Award and Okouchi Prize owing to the invention of stacked capacitor DRAM memory device. In addition, he was awarded IEEE Electronics Package Society (EPS) Award and 3DIC Pioneer Award by his pioneering works in 3D integration technology. He was also awarded Optoelectronic Technology Achievement Award from Japan Society of Applied Physics owing to his outstanding contributions to photonic technology. Furthermore, owing to his overall contribution to the progress of semiconductor technology he was awarded the National Medal Order of the Sacred Treasure, the National Medal with Purple Ribbon, and the Award of Ministry of Education, Culture, Sports, Science and Technology in Japan. He is an IEEE life fellow and a JSAP fellow.